

# PCI Model

**REVISION HISTORY**

NUMBER	DATE	DESCRIPTION	NAME
	v000.1		PL

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## **Contents**

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Project dates: October 2003 – November 2003 Developer: Victor Vengerov, Senior Software Engineer

A customer has to verify the behaviour of PCI core in his communication processor

During the project:

- API to communicate with Verilog model has been designed;
- A complete functional model of PCI state machine in C has been developed;
- Using the model, the customer identifies and fixes few problems in his PCI implementation;
- The model is stored for testing of future customer's products.

Total effort for the Development and Testing: 1.5 man-months

[Back to the list](#)

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